Attorney Docket No. YOR920030258US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): W. Rhee et al.
Docket No.: YOR920030258US1
Serial No.: 10/697,751
Filing Date: October 30, 2003
Group: 2816
Examiner: To Be Assigned

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature: /Ben Cheng/ Date: March 9, 2004

Title: Voltage-Controlled Delay Circuit Using Second-Order Phase Interpolation

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INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, Applicants' attorney wishes to bring to the attention of the Patent and Trademark Office the following documents listed on the accompanying Form PTO-1449. A copy of each listed document is enclosed.

1. S. Lee et al., "A 5 Gb/s 0.25 μm CMOS Jitter-Tolerant Variable-Interval Oversampling Clock/Data Recovery Circuit," ISSCC, Session 15, Gigabit Communications, pp. 463-465, February 2002.

2. J. Savoj et al., "A 10-Gb/s CMOS Clock and Data Recovery Circuit with a Half-Rate Linear Phase Detector," IEEE Journal of Solid-State Circuits, Vol. 36, No. 5, pp. 761-767, May 2001.

3. W. Rhee, "A Low Power, Wide Linear-Range CMOS Voltage-Controlled Oscillator," Proc. of IEEE, pp. II-85-II-88, May 1998.

It is believed that there is no fee due in conjunction with the filing of this Information Disclosure Statement. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **International Business Machines Corporation Deposit Account No. 50-0510** as required to correct the error.

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made, or as an admission that the information cited is considered to be material to patentability, or as a representation that no other material information exists.

Respectfully submitted,

Date: March 9, 2004

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FORM PTO-1449 (MODIFIED)

LIST OF PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	FILING DATE IF APPROPRIATE
___					

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	TRANSLATION YES	NO
___						

OTHER DOCUMENTS

EXAMINER INITIAL	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
___	1.	S. Lee et al., "A 5 Gb/s 0.25 μm CMOS Jitter-Tolerant Variable-Interval Oversampling Clock/Data Recovery Circuit," ISSCC, Session 15, Gigabit Communications, pp. 463-465, February 2002.
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Examiner _____ Date Considered _____

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.